Ben Lancaster

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EXPERIENCE

Senior CPU Design Engineer 2019 – present
Arm Ltd - Processor Design Group *Cambridge, UK*

- Micro-architecture specification and RTL design for A-class CPUs and multi-core clusters for client market targeting smartphones and large screen compute devices.
- Responsible for power/clock/reset logic for upcoming A-class CPUs featuring multiple power/clock/reset domains and crossings. Experience with CDC and RDC analysis.
- Extended CPU IP products to support ASIL B/D for automotive and safety critical applications (ISO 26262).
- Unit design lead for Memory system filtering unit, MPAM, and RAS units for an upcoming System IP.
- Contributions to design of a fully-coherent L3 System Level Cache using AMBA CHI and AXI5.
- Created automation flows for generating synthesizable SystemVerilog RTL from machine-readable specifications.
- Experience implementing AMBA interfaces including CHI, AXI, and APB.

Firmware Engineer, Internship 2016 - 2017
Spirent Communications - Positioning Group *Paignton, UK*

- Using Xilinx Virtex UltraScale+/Spartan FPGAs for RF signal generation (GNSS/VHF/UHF).
- Embedded C programming on Xilinx MicroBlaze and PIC16/24 micro-controllers.
- Implemented software algorithm for dynamic power attenuation and calibration using programmable DAC for GNSS RF signal generators.
- Controlling EEPROMs, LEDs, on-board fans, and other peripherals with I2C and SMBus.

EDUCATION

MSc (Eng) Embedded Systems Engineering, 1st 2018 – 2019
University of Leeds *United Kingdom*

- 1st, Final Project: Multi-core RISC SoC Design and Implementation for FPGAs.
- Courses include: FPGA Design for System-on-Chip, Digital Signal Processing for Communications, Embedded Microprocessor System Design, Circuit Analysis, Electronics for Medical Devices

BSc (Hons) Computer Science, 1st 2014 – 2018
University of Plymouth *United Kingdom*

- Top Final Year Student, Best Final Project, Revell Research Systems Price
- Final Project: FPGA-based 16-bit RISC soft-microprocessor (with IO & interrupts) and CFG Compiler

ADDITIONAL EXPERIENCE & AWARDS

- Best Final Project
- Top Final Year Student
- Dean's List 2015-2018 member
- Revell Research Systems Prize

OPEN-SOURCE PROJECTS & CONTRIBUTIONS

- Multi-core RISC CPU design. Fits up to 96 cores on Spartan-6 and Cyclone V FPGAs.
- 16-bit RISC ISA and CPU design. Written in Verilog and C compiler for a C-like programming language.
- Custom PCB with an ST Cortex M0 and debugging header. A 2-layer board for the Minispartan6+ FPGA development kit. Features an STM32F0 TSSOP processor, dual power supplies, I2C, ICSP, and LEDs.